1. $+13_{10} = 1101_{2TC} \rightarrow 00001101_{2TC}$

$+9_{10} = 1001 \rightarrow +9 = 00001001 \rightarrow -9 = 11110111_{2TC}$

$$
\begin{array}{ll}
00001101 & 13 \\
+\ 11110111 & +(-)9 \\
\hline
\text{\sout{X}}00000100 &
\end{array}
$$

Excluding the overflow bit $\rightarrow 00000100_2 = +4_{10}$

2. A combinational logic circuit's outputs are logical functions of its inputs while a sequential logic circuit's outputs are logical functions of its inputs **and** its current state (i.e. previous inputs)
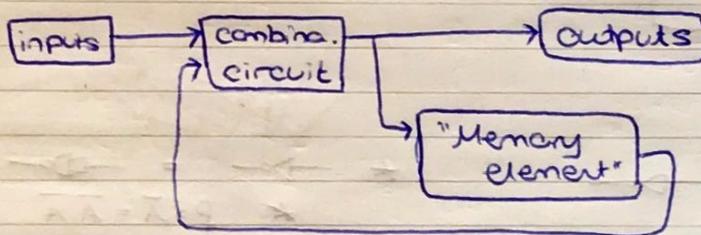

3.

A	B	A + B
0	0	0
0	1	1
1	0	1
1	1	1

4.

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

5. $f = \overline{A}.B + A.\overline{B}$
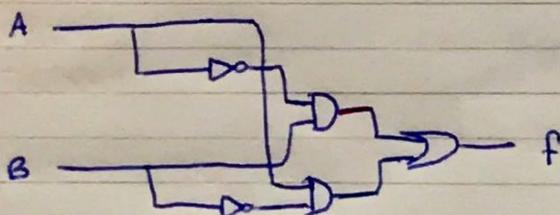
6.

A	B	A.B
0	0	0
0	1	0
1	0	0
1	1	1

7.

A	B	A+B
0	0	0
0	1	1
1	0	1
1	1	1

$$f = \overline{A}.B + A.\overline{B} + A.B$$
$$= \overline{\overline{A}.\overline{B}}$$

A	B	$\overline{A}.\overline{B}$	A.B
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	1
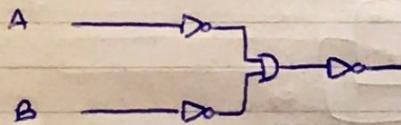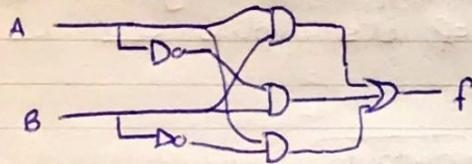
★ $p = \overline{A} = \overline{A.A}$
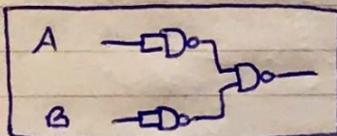
8.

C_{in}	A	B	C_{out}	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

9.
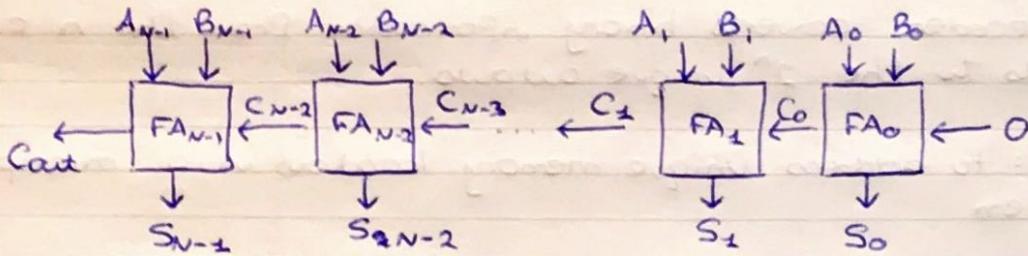
Each full adder has a carry in and a B and A input. The final carry out means there if 1 means that there has been an overflow (i.e. result generated is too large to fit on the bus).

10. By adding in a control line, Z: This should be exclusively ORed with each bit of B individually and is the C_{in} on the first full adder
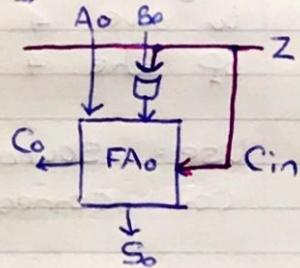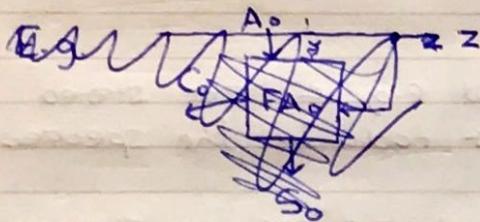
When $Z=0$: B is unchanged and the C_{in} is 0 so it acts as an adder ($S = A + B$)

When $Z=1$: the bits of B are inverted and C_{in} is 1 (i.e. 1 added to the sum) which is essentially forming the 2s complement of B, so it acts as a subtractor ($S = A + (-B)$)

11.
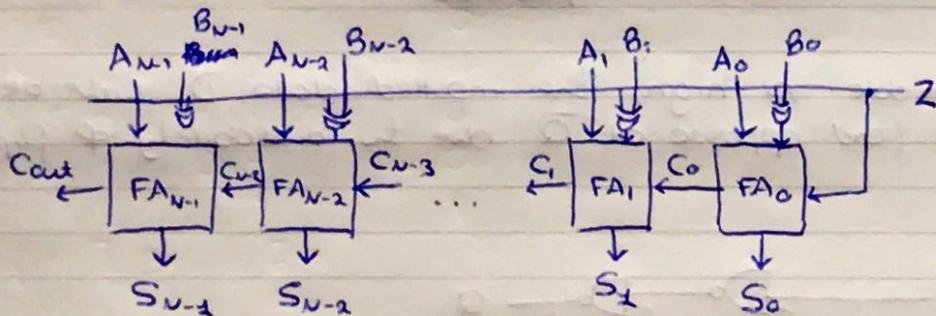
Carry out indicates the sign of the result now

12. A decoder converts binary information from the n coded inputs to the 2^n unique outputs.

Use: to address unique memory locations in a microprocessor system

↳ this is because each combination of input states has a unique output pin (i.e. memory location) which corresponds to the current input state

13. This outputs a selected input from multiple inputs using selection lines

E.g. a 4-1 multiplexer → this has 2 selection lines to give 4 options, each of which corresponds to one of the 4 input lines

Use: Source selection control e.g. a home stereo which can connect the iPod, CD or radio to the speakers (output)

14. A D-Type latch acts as a 1-bit 'memory storage' box. This is because the inputted data is only presented as the output when the enable line is high

When enable is 0, there is no change to the output as $\overline{0 \cdot D} = 1$. This is because both inputs to the 'flip-flop' NAND gates will be 1 so Q (output) will remain the same (due to flipflop ~~stability~~ feedback)

When enable is high, the inputted data, D, will be outputted at Q (and opposite at $\overline{Q}$ due to bistability of flipflop)

flip flop
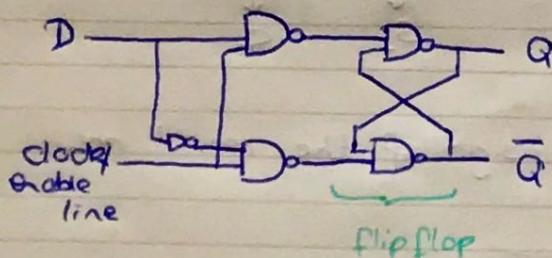
15.
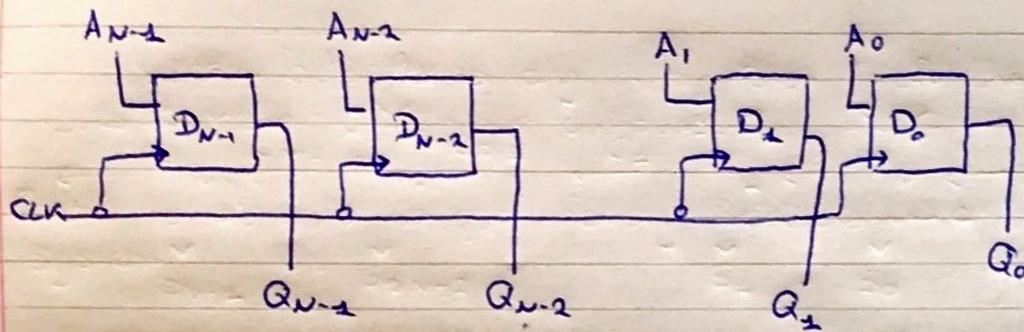
This is a parallel load register → each bit of A is loaded into an individual D-Type latch in the same clock cycle (i.e. same time)

This has a common clock → clock input signal goes to all the D-type latches at the same time

This circuit functions as a a N-bit memory system e.g. can store a N-bit number.

The clock pulse is provided by pushing a switch $(0 \rightarrow 1)$ or $(1 \rightarrow 0)$. However, this circuit only outputs Q when it's $0 \rightarrow 1$ ~~to~~ otherwise A will be stored. This is ~~because~~ because the D-type latches only respond to the rising edge.