# CS132 Quizzes - Digital Logic

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## 1 Subtract 9 from 13 in 8-bit wide two's complement.

13 = 00001101
9 = 00001001
flip bits
= 11110110
add 1
-9 = 11110111
13 + (-9) = 00001101 + 11110111 = (1)00000100
ignore the overflow
13 - 9 = 00000100 = 4.

## 2 Explain, with the aid of a diagram, the difference between combinatorial and sequential logic circuits.

A combinatorial logic will give the same results given the same inputs every time. There is no state of the circuit that can affect the output.
Whereas a sequential logic circuit can have a state which the circuit is in that could mean given the same input at different times could give a different result.

## 3 Show the truth table for an OR gate.

| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

Table 1: OR

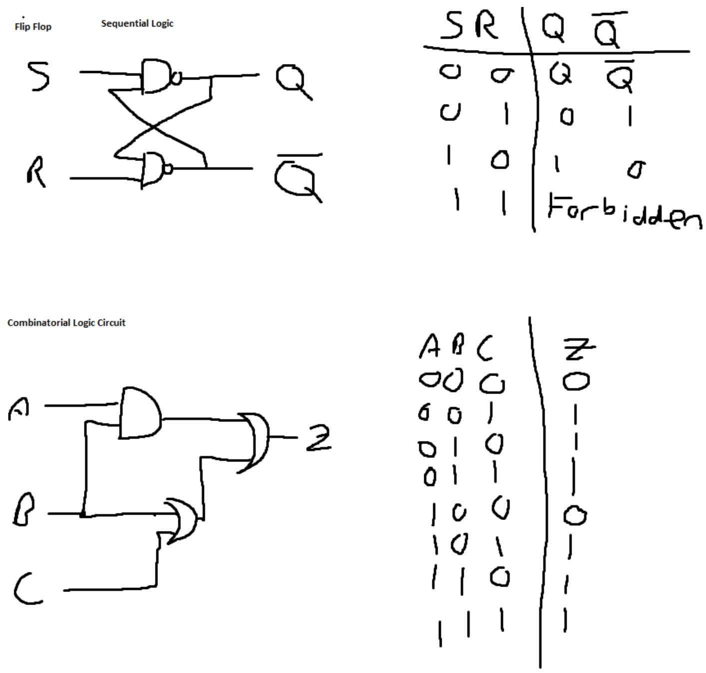


Figure 1: examples

## 4 Show the truth table for an XOR gate.

| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

Table 2: XOR

## 5 Design a circuit that implements the function of an EX-OR gate using only NOT, AND and OR gates.

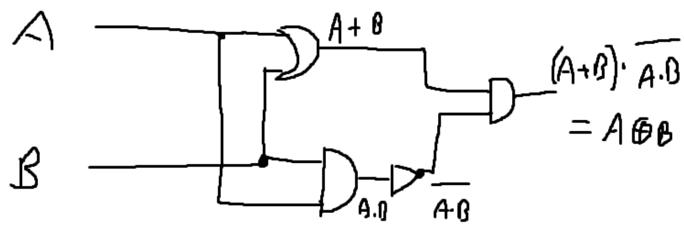


Figure 2: examples

## 6 Show the truth tables for a AND gate.

| A | B | Output |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Table 3: AND

## 7 Design a circuit that implements the function of an OR gate using only NAND gates.

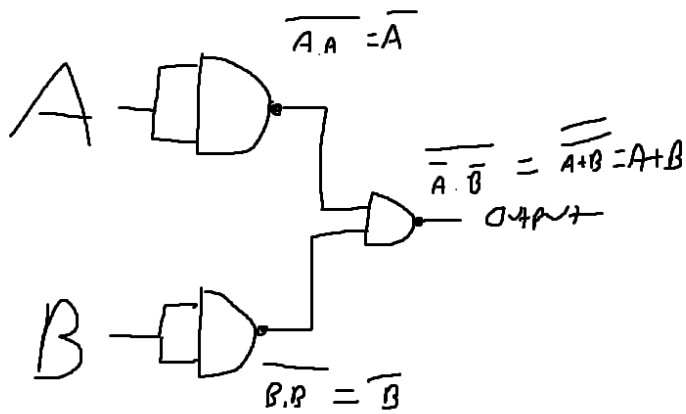


Figure 3: examples

# 8 Show the truth table for a 1-bit full adder.

| A | B | Carry In | Sum | Carry Out |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

Table 4: 1-bit full adder truth table

# 9 Design am N-bit Full Adder circuit.

# 10 Explain how an N-bit Full Adder circuit can be modified to form an N-bit subtractor circuit.

We can use the fact that a-b = a+(-b) and have a mode control line (z) that can turn b into -b.

This can be done by flipping the bits of b and then adding 1. So we can

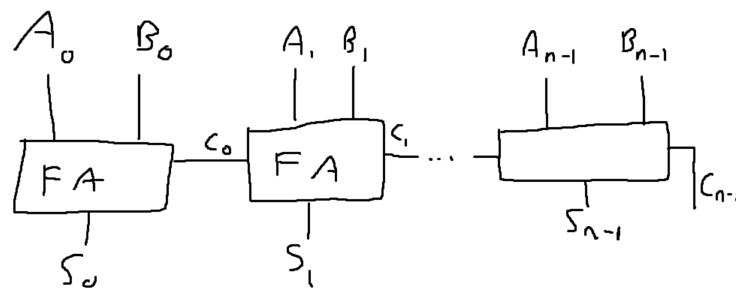


Figure 4: examples

XOR each B in b with the control line. When z is high the bits will be flipped, otherwise they will remain the same. Then to add the extra bit we can just use z as the Carry In to the first 1-bit full adder.

## 11 Design an N-bit Subtractor circuit.

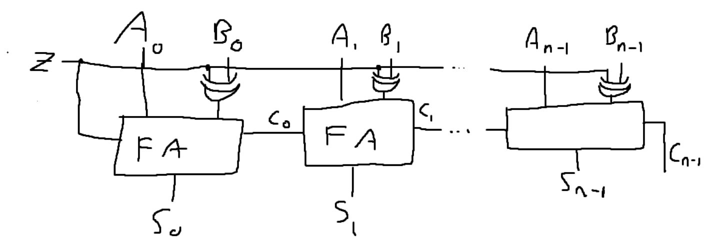


Figure 5: examples

## 12 Explain the function of a decoder, giving an example of where a decoder might be used.

A decoder turns n inputs into $2^n$ outputs. A decoder turns one of the outputs on determined by the binary value of the input.
e.g. for an active-low decoder the truth table will be as follows:

| $x_0$ | $x_1$ | $y_0$ | $y_1$ | $y_2$ | $y_3$ |
|---|---|---|---|---|---|
| 0 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |

Table 5: decoder

Decoders are often used to address unique memory locations in a microprocessor system

# 13 Explain the function of a multiplexer, giving an example of where a multiplexer might be used.

A multiplexer turns n inputs into 1 output, determined by some control modes. A multiplexer turns the output into one of the inputs determined by the control modes.
multiplexer truth table for a 4-1 multiplexor (inputs are $x_0, x_1, x_2, x_3$ and control signals are $S_0, S_1$):

| $S_0$ | $S_1$ | output |
|---|---|---|
| 0 | 0 | $x_0$ |
| 0 | 1 | $x_1$ |
| 1 | 0 | $x_2$ |
| 1 | 1 | $x_3$ |

Table 6: multiplexer

multiplexers are used for source selection control e.g. home stereo control.

# 14 Explain, using an appropriate truth table or circuit diagram, the operation of a D-Type latch.

A D-Type latch is essentially 1 bit of memory. Depending on the current state of the D-Type latch the input to the d-type latch will alter the output.
Below is the circuit diagram of a D-Type Latch

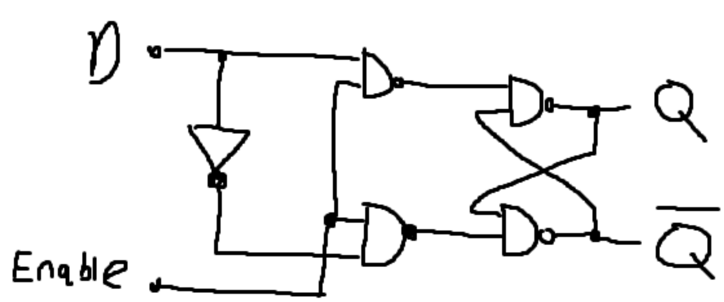


Figure 6: d-type latch

Below is the truth table for the d-type latch:

| Enable | D | Q | $\overline{Q}$ |
|---|---|---|---|
| 0 | 0 | Q | $\overline{Q}$ |
| 0 | 1 | Q | $\overline{Q}$ |
| 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 |

Table 7: D-Type latch

# 15 Show how D-type latches can be arranged to form an N-bit register, explaining the function of your circuit.

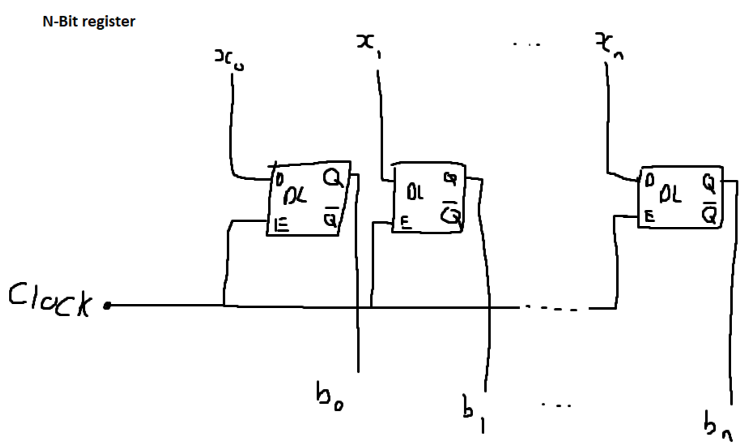


Figure 7: d-type latch

make note this diagram assumes the D-type latches are rising edge triggered.